DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING,
MANIPAL UNIVERSITY JAIPUR
M. Tech. in VLSI & EMBEDDED SYSTEM DESIGN (VESD)

FIRST SEMESTER

ECE6104: EMBEDDED SYSTEMS [4 0 0 4]

Introduction: Overview of embedded systems, embedded system design challenges, common design metrics and optimizing. Survey of different embedded system design technologies & trade-offs. Embedded microcontroller cores, embedded memories, Examples of embedded systems. Architecture for embedded system, High performance processors: The ARM Design Philosophy, Embedded System Hardware, Embedded System Software. ARM Processor Fundamentals: Architecture Revisions, ARM Processor Families, Introduction to the ARM Instruction Set: Data Processing Instructions, Branch Instructions, Load- Store Instructions, Software Interrupt Instruction, Program Status Register Instructions, Introduction to the Thumb Instruction Set, ARM Organization and Implementation, with example, Programming with ARM: Programming loops, Character coded data, Code conversion, and Arithmetic examples. Technological aspects of embedded systems: interfacing between analog and digital blocks, signal conditioning, Digital signal processing, Subsystem interfacing, interfacing with external systems. Real time programming languages and operating systems for embedded systems: RTOS requirements, kernel types, scheduling, context switching, latency, inter-task communication and synchronization, Case studies.

References:

1. Muhammad Ali Mazidi, *ARM Assembly Language Programming Architecture: Volume (ARM books*), MicroDigitalEd.com, 2016.
2. Yifeng Zhu*, Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C*, E-Man Press LLC; 2nd ed. edition (15 October 2015).
3. S. Furber, *ARM System-on- Chip Architecture,* Second Edition, Pearson Education, 2000.
4. J. R. Gibson, *ARM Assembly Language-an Introduction*, Dept. of Electrical Engineering and Electronics, The University of Liverpool, 2007.
5. A. N. Sloss, Dominic Symes, Chris Wright, *ARM System Developer's Guide,* Elsevier, 2004.
6. Jack Ganssle, *The Art of Designing Embedded Systems, Elsevier,* 1999.
7. R. Gupta, *Co-synthesis of Hardware and Software for Embedded Systems*, Kluwer 1995.

ECE6105: ADVANCE DIGITAL VLSI DESIGN [4 0 0 4]

VLSI design methodologies: VLSI design flow, design hierarchy, Concepts of Regularity, Modularity and Locality, VLSI design styles, Design Quality and Computer Aided Design. MOS Transistor theory: Operation and characteristics, Threshold voltage, Body effect, Sub threshold conduction, Channel length modulation, mobility variation, Tunnelling, Drain punch through and Hot electron effect; MOS models, small signal AC characteristics; CMOS inverter, β_n/β_p ratio, noise margin, static load MOS inverters, tristate inverter; Advantages of CMOS over NMOS, CMOS/SOI technology, CMOS/Bulk technology, latch up in bulk CMOS and its prevention. Principles of Digital VLSI Design using CMOS: Principles of circuit design using pass transistors and transmission gates; Combinational Logic circuit design using CMOS logic; Sequential logic Circuit design using CMOS, Flip Flops, synchronous sequential circuits and clocked storage elements. Basic circuit concepts and performance estimation: Introduction, Resistance Estimation Capacitance Estimation and switching characteristics of CMOS gates; Transistor Sizing, Power dissipation, Sizing

Routing Conductors, Design Margins and Reliability. Dynamic CMOS logic and clocking: Introduction, static CMOS design, Pseudo NMOS circuits, Domino CMOS structure and design, Charge sharing, clocking, clock generation and distribution. Semiconductor memories & I/O circuits. Various types of memories and their working.

References:

1. J. M Rabaey, *Digital Integrated Circuits*, (3e), Prentice Hall India, 2003.
2. W. N. & K. Eshraghian, *Principles of CMOS VLSI Design*, (2e), Addison Wesley, 1993.
3. S. M. Kang & Y. Leblebici, *CMOS digital Integrated circuits design and analysis* , (3e), Tata McGraw Hill, 3rd edition, 1996.

ECE6106: DIGITAL SYSTEM DESIGN USING VERILOG [4 0 0 4]

Review of logic design fundamentals.Design of Synchronous and asynchronous Circuits, Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs Introduction to Verilog: variables, constant, operators, delays, test bench, Digital system design options and trade-offs, Design methodology and technology overview, High Level System Architecture and Specification: Behavioral modeling, simulation and synthesis. Digital Design Using ROMs, PALs and PLAs , Arithmetic Circuits: BCD Adder, other adders, State graphs for control circuits, shift and add multiplier, Array multiplier, different multipliers, Binary divider. Introduction to FSM, State equivalence and machine minimization. Fundamental mode model, Flow table, State reduction, Minimal closed covers, Races, Cycles and Hazards. State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller. Overview of FPGA architectures and technologies, Logic block architecture, Input and Output cell characteristics, clock input, Timing, Power dissipation, Programmable interconnect, Applications

References:

1. Prakash Rashinkar Peter Paterson & Leena Singh, *SoC Verification Methodology and Techniques*, Kluwer Academic, 2001.
2. William K. Lam, *Design Verification: Simulation and Formal Method based Approaches*, Prentice Hall, 2005.
3. Pong P. Chu, *FPGA Prototyping By Verilog Examples*, John Willy, 2001.
4. Thomas & Moorby's, *The Verilog Hardware Description Language*, Kluwer Academic, 1998.

PROGRAM ELECTIVE-I

ECE6148: VLSI PROCESS TECHNOLOGY [3 0 0 3]

Material Properties: Physical properties, Crystal structure, Miller indices, Packing Density, Defects, Dislocation. Crystal Growth: Silicon Crystal Growth - Czochralski and Float Zone Technique, Distribution of dopants, Segregation/Distribution coefficient. Silicon Oxidation: Thermal Oxidation process- Kinetics of Growth, Deal-Grove Model, Impurity Distribution, Masking properties. Photolithography: Photo resists, Lift Off technique, Optical Lithography, Next generation lithography .Diffusion: Basic diffusion process- Fick's first and second law, Pre-deposition and drive-in diffusion, Diffusion profile for various dopants, Lateral Diffusion. Ion Implantation: Range, straggle, ion stopping, ion Channeling, RTA. Etching: Wet and dry etching- Plasma fundamentals; Film Deposition: PECVD, and Epitaxy Metallization: evaporation and sputtering; Realizing resistor, capacitor, diode, BJT, MOSFET, CMOS structures, Twin Tub process, High - k Dielectrics, electro-migration. Single and Double Damascene process. IC assembly techniques: Dicing, Bonding and types of packaging & packaging process.

References:

1. S. M. Sze, "VLSI Technology", Second Edition, McGraw Hill, 1988.

2.S. K. Gandhi, “VLSI Fabrication Principles”, Second Edition, John Wiley & Sons, 1983.
3S. A. Campbell, “The Science & Engineering of Microelectronic Fabrication”, Second Edition, Oxford University Press, 2005.
4.G. S. May & S. M. Sze, “Fundamentals of Semiconductor Fabrication”, Wiley Student edition, 2004.

ECE6149: FPGA ARCHITECTURES & APPLICATIONS [3 0 0 3]

Finite State Machines: Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronous sequential design of Moore, Melay Machines, Top down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine. Algorithmic State Machine- An Algorithm with inputs, digital solution, Implementation of traffic light controller, ASM charts, Design Procedure for ASMs, Data path and Control design. FPGAs Architecture: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA’s FLEX 8000/10000 FPGAs. Introduction to advanced FPGAs: Xilinx Virtex and ALTERA Stratix. Logic block and architecture, Introduction to standard libraries of Xilinx, System Level Design: Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs. System level design using mentor graphics/Xilinx EDA tool (FPGA Advantage/Xilinx ISE), Design flow using FPGAs. Case studies: Design considerations using FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

References:

1. Navabi , *Analysis and modeling of digital systems*, McGraw Hill, 1998.
2. S. Brown & Z. Vransesic , *Fundamental of digital Logic with Verilog design*, TMH, 2000.
3. J. Bhaskar, *A VHDL Primer*, Addison Wesley, 2000.
4. Perry, *Modeling with VHDL*, McGraw Hill, 1994.
5. Trimberger, *Field Programmable Gate Array Technology*, Kluwer Academic Publications, 1994.

ECE6150: HIGH SPEED IC DESIGN [3 0 0 3]

Non Clocked Logic Styles: Static CMOS, DCVS logic, Non-Clocked Pass-Gate Families. Clocked Logic Styles- Clocked Logic Styles, Single-Rail Domino Logic Styles, Alternating-Polarity Domino Approaches, Dual-Rail Domino Structures, Latched Domino Structures, Clocked pass Gate Logic. Circuit Design Margining And Design Variability- Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise. Latching Strategies- Latching Strategies, Basic Latch Design, Latching Differential Logic, Race Free Latches for Pre-charged Logic, Asynchronous Latch Techniques. Interface Techniques- Signalling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design Clocking Styles- Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques, Single Phase Clocking & Multiphase Clocking. Slack Borrowing & Time Stealing: Introduction, Slack Borrowing, Time stealing.

Reference books:

1. Kerry Bernstein, Keith M. Carrig, *High Speed CMOS Design Styles*, Kluwer Academic Publishers, 2002.
2. Evan Sutherland, Bob Stroll, David Harris, *Logical Efforts Designing Fast CMOS Circuits* , Kluwer Academic Publishers, 1999.
3. J. M Rabaey, *Digital Integrated Circuits*, (3e), Prentice Hall India, 2003.

ECE6151: ADVANCED SENSOR AND ACTUATORS [3 0 0 3]

Measurement Terminology: Input and output, range, accuracy, precision, resolution, sensitivity, linearity, repeatability, reproducibility, calibration and traceability, Testing, quality assurance and safety. Transducers and sensors: Sensors and transducers: Temperature sensors, resistive sensors, capacitive sensors, electrostatic sensors, piezoelectric sensors, and MEMS. Optical sensing techniques: Common electromagnetic sensors, IR sensors, passive IR sensors, photo-resistive sensors, photovoltaic sensors, photodiodes, photoelectric detectors, solid state lasers, CCD and CMOS sensors. Smart Sensors: Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing , Data Communication, Standards for Smart Sensor Interface, The Automation Sensors Applications: On-board Automobile Sensors (Automotive Sensors), Home Appliance Sensors, Aerospace Sensors, Sensors for Manufacturing, Sensors for environmental Monitoring. Actuators: Pneumatic and Hydraulic Actuation Systems, Actuation systems, Pneumatic and hydraulic systems, Directional Control valves, Pressure control valves , Cylinders, Servo and proportional control valves , Process control valves , Rotary actuators Mechanical Actuation Systems. Electrical Actuation Systems, Electrical systems, Solid-state switches Solenoids, D.C. Motors, A.C. motors, Stepper motors. Emerging Topics: Introduction to sensor networks, sensor fusion, soft and intelligent sensors. System on module, Virtual instrumentation, intelligent instrumentation, Fault tolerance, Real time systems introduction, reference model, scheduling approaches.

References:

1. D. Patranabis, Sensors and Transducers, PHI Learning Private Limited.
2. W. Bolton, Mechatronics, Pearson Education Limited.
3. D. Patranabis , Sensors and Actuators, 2nd Ed., PHI, 2013.

ECE6152: CRYPTOGRAPHY AND CRYPTO CHIP DESIGN [3 0 0 3]

BASIC CONCEPTS: Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism in OS, Targets: Hardware, Software, Data communication procedures. Threats to Security: Physical security, Biometric systems, monitoring controls, Data security, systems, security, Computer System security, communication security. Encryptions Techniques: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication and Hash Algorithm: Authentication requirements and functions secure Hash Algorithm, NDS message digest algorithm, digital signatures, Directory authentication service

Firewalls and Cyber laws: Firewalls, Design Principles, Trusted systems, IT act and cyber laws, Virtual private network. Future Threats to Network: Recent attacks on networks, Case study.

APPLICATIONS: AES algorithm, Crypto chip design: Implementation of DES, IDEA AES algorithm, development of digital signature chip using RSA algorithm.

References:

1. William Stalling, *Cryptography and Network Security*, Pearson Education, 2005

2.Charels P. Pfleeger, *Security in Computing*, Prentice Hall, 2006

3.Jeff Crume, *Inside Internet Security*, Addison Wesley, 2000.

ECE6153: ARM BASED SYSTEM DEVELOPMENT [3 0 0 3]

Introduction to microcontroller: Review of different types of microprocessors and microcontrollers, History of Micro controllers, Embedded versus External memory devices, Microcontroller survey, CISC and RISC Microcontrollers, Harvard and von Neumann Architecture. The ARM Design Philosophy, Embedded System Hardware, Embedded System Software. ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts, and the Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families, Introduction to the ARM Instruction Set: Data Processing Instructions, Branch Instructions, Load-Store Instructions, Software Interrupt Instruction, Program Status Register Instructions, Loading Constants, ARMv5E Extensions, Conditional Execution, Writing simple assembly language programs, Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM - Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction. ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, and The ARM coprocessor interface.

Memory Hierarchy: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management. Programming with ARM: Programming loops, Character coded data, Code conversion, and Arithmetic examples.

References:

1. Muhammad Ali Mazidi, ARM Assembly Language Programming Architecture: Volume (ARM books), MicroDigitalEd.com, 2016.
2. Yifeng Zhu, Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C, E-Man Press LLC; 2nd ed. edition (15 October 2015).
3. S. Furber, ARM System-on- Chip Architecture, Second Edition, Pearson Education, 2000.
4. J. R. Gibson, ARM Assembly Language-an Introduction, Dept. of Electrical Engineering and Electronics, The University of Liverpool, 2007.
5. A. N. Sloss, Dominic Symes, Chris Wright, ARM System Developer's Guide, Elsevier, 2004.

ECE6154: MEDICAL ELECTRONICS AND INSTRUMENTATION [3 0 0 3]

Human body subsystems : brief description of neuronal, muscular, cardiovascular and respiratory systems; their electrical, mechanical and chemical activities. Cardiovascular system: measurement of blood pressure, blood flow, cardiac output, cardiac rate, heart sounds; electrocardiograph, phonocardiograph, plethysmograph. Respiratory system: measurement of gas volume, flow rate, carbon-dioxide and oxygen concentration in exhaled air. Electrical activity in neuromuscular system and brain: neuron potential, muscle potential, electromyography, brain potentials, electroencephalograph. Medical imaging: fundamentals of imaging, computed tomography, mri, nuclear medicine, single photon emission computed tomography, pet, ultrasonography, electrical impedance, tomography. Medical safety: electrical safety, electrical safety codes and standards; radiation safety, chemical safety, biological safety, fire and explosive safety, environmental safety. Assisting and therapeutic equipment's: pacemakers, defibrillators, ventilators , nerve and muscle stimulators, diathermy, heart-lung machine, infant incubators, audio meters, dialyzers.

References:

1. Webster JG (Ed.), Medical Instrumentation, Application and Design, Wiley India.
2. Carr JJ and Brown JM, Introduction to Biomedical Equipment Technology, Pearson Education.
3. Waugh A and Grant A, Ross and Wilson Anatomy and Physiology in Health and Illness, Elsevier.
4. Webster JG (Ed.), Encyclopedia of Medical Devices and Instrumentation, Vols. 1-4, Wiley.
5. Bronzino JD (Ed.), The Biomedical Engineering Handbook, CRC Press

ECE6155: MICROCONTROLLER AND EMBEDDED SYSTEMS- I [3 0 0 3]

Introduction to Computing, The AVR Microcontroller: History and Features, AVR Architecture and Assembly Language Programming Branch, Call, and Time Delay Loop, AVR 1/0 Port Programming, Arithmetic, Logic Instructions, and Programs AVR Advanced Assembly Language Programming AVR, Programming in C, AVR Hardware Connection, Hex File, and Flash Loaders AVR Timer Programming in Assembly and C, AVR Interrupt Programming in Assembly and C AVR Serial Port Programming in Assembly and C LCD and Keyboard Interfacing ADC, DAC, and Sensor Interfacing, Relay, Optoisolator, and Stepper Motor Interfacing with AVR Input Capture and Wave Generation in AVR, PWM Programming and DC Motor Control in AVR SPI Protocol and MAX722 I Display Interfacing, 12C Protocol and DS 1307 RTC Interfacing.

References:

1. Muhammad Ali Mazidi, Sarmad Naimi, Sepehr Naimi, AVR Microcontroller and Embedded Systems : Using Assembly and C, Pearson education India, 2013.
2. Dhananjay Gadre, Programming and Customizing the AVR Microcontroller, McGraw Hill Education, 2017.

3. Daniel J. Pack and Steven F. Barrett , Atmel AVR Microcontroller Primer: Programming and Interfacing, Second Edition, Morgan & Claypool Publishers, 2012.
4. David E Simon, An embedded software primer, Pearson education Asia, 2001
5. Jack Ganssle, The Art of Designing Embedded Systems, Newnes, 1999.

EC6132: EMBEDDED SYSTEM DESIGN LAB-I [0 0 2 1]

This lab will enable the students to program, simulate and test the 8085, 8051, PIC 18 and ARM processor based circuits and their interfaces. This lab provides a platform for various projects using embedded.

ECE6133: SYSTEM DESIGN USING FPGA LAB [0 0 2 1]

This lab give exposure to simulation & synthesis software using Xilinx Vivado. This lab aims to implement various digital circuit like combination, Sequential, FSM, ASM etc. using Verilog HDL & synthesis. Test benches for various circuits for delays. Use of FPGA boards to synthesis their codes is also a part of this lab.

ECE6170: SEMINAR [0 0 2 1]

Student has to present a seminar on any of the recent advances in VLSI/embedded systems engineering as per his choice and research interest (with reference to IEEE and other reputed journals, recent books and white papers in the related field).

The topic selected for the presentation would require the approval of the instructor. Student would be required to submit a report as per the format provided by the department.

SECOND SEMESTER

ECE6204: ADVANCED MICROCOMPUTER SYSTEMS & INTERFACING [4 0 0 4]

Introduction Microprocessors, Classes of Processors, Pipeline & Replication, Flynn's Taxonomy, Basic Program Execution Model, Programmers Model - 8086,80286,80386,80486, 8086-80486 Instruction Encoding Schemes, Data Transfer Instructions - Data copy, Awapping, Stack Based Operations, Data Manipulation Instructions- Arithmetic & Logic Operations, String Operations, Shift Rotate Operations, Introduction to MASM- Assembler Directives, Program Control Instructions - Branching, Subroutines, Software Interrupts Macro, Pin Out of 8086 Minimum & Maximum Mode of Operation, Memory Organization - Real & Protected Mode, Memory Interfacing & Banking, x86 Interfacing to I/O devices, Buses.

References:

1. Barry B Brey, *The Intel Microprocessors* .Pearson,(8e) 2009.
2. Douglas V Hall, *Microprocessor and Interfacing*, TMH, (2e),2010.

ECE6205: VLSI PHYSICAL DESIGN & AUTOMATION [4 0 0 4]

VLSI physical Design: VLSI design cycle, Trends in physical design cycle. Basic algorithms: Basic terminology, Complexity Issues and NP-Hardness, Graph algorithms, computational Geometry algorithms, Basic data structures, Algorithms for different classes of graphs in physical. Circuit partitioning: Partitioning metrics, Problem formulation, Move-Based Partitioning Methods, Simulated Annealing and evolution, Multilevel Partitioning and clustering. Floorplanning and placement: Problem formulation and cost metrics, Graph representation of floorplans, Floorplan sizing, Cluster growth, Simulated Annealing based floorplan and placement algorithms, Partitioning based placement algorithms, Pin assignment. Grid Routing: Gl obal Routing, Detailed routing, Problem formulation and ordering of nets, Maze routing algorithms, Line search algorithms, Channel routing, Multi-layer channel routing, Switchbox routing, over the cell routing, via minimization, clock and power routing. Layout Compaction: Problem formulation, 1-D compaction, 1½ and 2D compaction, Virtual grid based compaction, Hierarchical compaction.

References:

1. N. A. Sherwani, *Algorithms for VLSI Physical Design Automation*, (3e), Kluwer Academic Publishers, 2002.
2. S. M .Sait, H. Youssef, *VLSI Physical Design Automation: Theory and Practice*, World Scientific Publishing, 1999.
3. S.H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley & Sons, 2008.
4. S. K. Lim, *Practice Problems in VLSI physical design Automation*, Springer, 2008.
5. C. J. Alpert, D. P. Mehta, S. S. Sapatnekar, *Hand Book of Algorithms of Physical design Automation*, CRC press, 2009.

ECE6206: ANALOG CMOS IC DESIGN [4 0 0 4]

Review of MOS Transistor operation models and equivalent circuits for low and high frequency. Single-Stage Amplifiers: CS, CG, CD, Cascode and folded cascode amplifiers, Differential Amplifiers: Common mode, differential mode response analysis and gain calculation. Passive and Active Current Mirrors: Cascode current mirror, current mirror as an active device, Frequency response of CS, CG, CD amplifiers, Miller effect for frequency response of amplifiers, Feedback amplifiers, Theory and design of MOS Operational Amplifier, Stability of operational amplifiers: Negative feedback amplifier using an integrator; Frequency and time domain behavior; Loop gain and its implications; Negative feedback amplifier realization, Effect of multiple poles, Negative feedback systems with multiple poles and zeros in the forward path, Loop gain-Bode plot and time domain interpretation; Significance of 60 degree phase margin, Frequency compensation of operational amplifiers: Realizing a multi stage op-amp frequency compensation-miller op-amp, feedforward compensated op-amp; unity gain compensation, slew rate. Reference voltage and current generators, Phase locked loops. Analog-to-Digital and Digital-to-Analog Converters

References:

1. N. A. Sherwani, *Algorithms for VLSI Physical Design Automation*, (3e), Kluwer Academic Publishers, 2002.
2. S. M .Sait, H. Youssef, *VLSI Physical Design Automation: Theory and Practice*, World Scientific Publishing, 1999.
3. S.H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley & Sons, 2008.
4. S. K. Lim, *Practice Problems in VLSI physical design Automation*, Springer, 2008.

PROGRAM ELECTIVE-II

ECE6255: VLSI TESTING & VERIFICATION [3 0 0 3]

Physical Faults and their modelling: Stuck at Faults, Bridging Faults; Fault collapsing; Fault Simulation: Deductive, Parallel and Concurrent Fault Simulation. Critical Path Tracing. ATPG for Combinational Circuits: D-Algorithm, Boolean Differences, PODEM Random, Deterministic and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage. ATPG for Sequential Circuits: Time Frame Expansion; Controllability and Observability Scan Design, Boundary Scan for Board Level Testing; Memory Testing: Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests; Delay Faults. PLA Testing: Cross Point Fault Model and Test Generation. Compression Techniques: General Aspects of Compression Techniques; Ones-Count, Transition Count and Parity Check Compression; Syndrome Testing; Signature Analysis; Built-In-Self-Test (BIST) Concept: Test-Pattern generation for BIST; Specific BIST Architecture; Introduction to Built-In-Self-Repair (BISR) Approaches. System Level Diagnosis & Repair: Introduction; Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Code; Verification: Design verification techniques based on simulation, analytical and formal approaches; Functional Verification, Timing Verification, Formal Verification, Bas ics of Equivalence Checking and model checking, Hardware Emulation.

References:

1. M. Abramovici, M. A. Breuer, & A.D. Friedman, *Digital Systems Testing and Testable Design,* Piscataway, New Jersey: IEEE Press, 1994.
2. M. L. Bushnell and V. D. Agrawal, *Essentials of testing for digital, memory and mixed-signal VLSI circuits*, Boston: Kluwer Academic Publishers, 2000.
3. P.K. Lala, *Fault Tolerant & Fault Testable hardware Design,* BS Publications, 1998

ECE6256: CAD TOOLS FOR VLSI [3 0 0 3]

Semiconductor device fabrication techniques: NMOS, PMOS and CMOS; Stick diagram and Design rules for MOS Circuits; PLA circuit implementation; Semiconductor TCAD Tool. Basic of Graph Theory: Ty pes of graph; Graph optimization problems and Algorithms; Introduction to PLDs, Types, Boolean logic implementation, Classification of FPGA, Switching technology. Cell-library binding: Subject graph, Pattern Graph and simple library design; Tree based covering using Dynamic programming and using Automata; Look-up table and Anti-fuse based FPGAs; State diagram, state flow sequencing graph. Architectural synthesis: strategies for architectural optimizations, Area/ Latency, Cycle-time/Latency and Cycle-time/Area optimizations; Model for scheduling problems, scheduling with resource and without resource constraints.Two level combinational logic synthesis and optimization: Exact and Heuristic method, Sequential logic Optimization.

References:

1. Stephen Trimberger, *Introduction to CAD for VLSI*, Kluwer Academic, 2002
2. G. De Michelll , “Synthesis and Optimization of Digital Circuits”, Tata-McGraw Hill, New Delhi,1994.
3. G. D. Hachtel, F. Somenzi, “Logic Synthesis and Verification Algorithm”, Kluwer Application Specific ICs Academic Publication, Boston, 2002.

ECE6257: SYSYTEM ON CHIP DESIGN [3 0 0 3]

System On Chip Design Process: SoC Design flow waterfall vs spiral, top-down vs Bottom up. Specification requirement, Types of Specification , System Design process, System level design issues, Soft IP Vs Hard IP, Design for timing closure, Logic design issue Verification strategy, On-chip buses and interfaces, Low Power, Manufacturing test strategies. Macro Design Process: Top level Macro Design, Macro Integration, Soft Macro products, Developing hard macros, Design issues for hard macros, Design ,System Integration with reusable macros. SoC Verification: Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification and Static net list verification. Verification architecture, Verification components, Introduction to VMM, OVM and UVM. Design of Communication Architectures for SoCs: On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures, Communication architecture tuners, and Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification.

References:

1. Prakash Rashinkar Peter Paterson & Leena Singh, *SoC Verification Methodology and Techniques* , Kluwer Academic, 2001.
2. William K. Lam, *Design Verification: Simulation and Formal Method based Approaches*, Prentice Hall, 2005.
3. Dirk Jansen, *The EDA Handbook*, Kluwer Academic, 2010.

ECE6258: MIXED SIGNAL IC DESIGN [3 0 0 3]

Introduction: Analog and discrete-time signal processing, analog integrated continuous-time and discrete-time filters. Filter Design: Analog continuous-time filters: passive and active filters. Basics of analog, discrete-time filters and Z-transform. Switched Capacitor Filters: Basic switched capacitor, Non-idealities in switched-capacitor filters. Switched-capacitor filter architectures, Switched-capacitor filter applications. Data Converters: Basics of Data Converters, DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Successive approximation ADCs, Flash ADC & Pipeline ADC, Basics of DAC.PLL: Basic of PLL, Analog PLL & Digital PLL. Dynamicsof simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Mixed Signal Layout, applications.

References :

1. R. J. Baker, CMOS: Mixed-Signal Circuit Design, (2Ee Wiley, 2002.
2. Behzad Razavi, *Design of analog CMOS integrated circuitsS, (*3e) McGraw-Hill, 2003.
3. D. Johns & K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 1997.
4. R.v.de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, Springer, 2003

ECE6259: LOW POWER VLSI DESIGN [3 0 0 3]

Need for Low Power VLSI chips, Sources of power dissipation in Digital Integrated circuits. Emerging low power approaches, Hierarchical Low Power Design Methodologies. Device & Technology Impact on Low Power: Physics of power dissipation in CMOS devices; Dynamic and static power dissipation, Transistor sizing & gate oxide thickness; Impact of technology Scaling and Device innovation. Power estimation, Simulation and Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis. Circuit level Power reduction techniques: Power consumption in circuits; Design of Flip Flops and Latches; Low Power Dynamic logic families & adiabatic logic families. Logic level Power reduction techniques: Gate reorganization, pre-computation logic, signal gating, logic encoding, state machine encoding, reduction of power in address and data buses. Low power Architecture and Systems: Power and performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. Low power Clock Distribution: Power dissipation in clock distribution, Single driver versus Distributed buffers, Zero skew versus Tolerable skew, chip and package co design of clock network. Algorithm and Architectural level Methodologies: Introduction, design flow, Algorithmic level analysis and optimization, Power aware software designs, Architectural level estimation and synthesis.

References:

1. G. K. Yeap, *Practical Low Power Digital VLSI Design*, (1e), Kluwer Academic, 2002.
2. Rabaey, Pedram, *Low power design methodologies*, (1e), Kluwer Academic, 1997.
3. K. Roy, S. Prasad, *Low Power CMOS VLSI Circuit Design*, (1e), Wiley, 2000.
4. Kiat, Samir S, R. S. Yeo, W. L. Goh, *CMOS/BiCMOS ULSI Low Voltage Low Power*, (1e), Pearson, 2002.

ECE6260: MACHINE LEARNING [3 0 0 3]

Introduction and Basic Concepts. Supervised Learning Setup. Linear Regression. Weighted Least Squares. Overfitting and complexity, Overfitting and complexity, Logistic Regression. Newton’s Method. Perceptron. Exponential Family. Generalized Linear Models. Gaussian Discriminant Analysis. Naive Bayes. Laplace smoothing. Laplace Smoothing. Support Vector Machines. SVM. Kernels. Bayesian Learning and Decision Trees, Ensemble methods: Bagging, random forests, boosting, unsupervis ed learning: clustering, k-means, and hierarchical agglomeration, Graphical Models, Learning Theory and Expectation Maximization, Introduction to Reinforcement Learning.

References:

1. T . Hastie, R. Tibshirani, J. Friedman, *The Elements of Statistical Learning*, 2e, Springer,2008.

2. Christopher Bishop, *Pattern Recognition and Machine Learning*. 2e.Springer,2006

ECE6261: EMBEDDED WIRELESS SENSOR NETWORKS [3 0 0 3]

ISSUES IN AD HOC WIRELESS NETWORKS: Medium Access Scheme-Routing-Multicasting- Transport Layer Protocols-Self Organization-Security-Addressing and Service Discovery Energy management- Scalability-Deployment Considerations, Ad Hoc Wireless Internet. Sensor Networks Comparison with Adhoc wireless networks- Challenges for wsns, Difference between sensor networks and Traditional sensor networks – Types of Applications Enabling Technologies for Wireless Sensor Networks ,Single Node Architectures – Hardware Components , Energy Consumption of Sensor Nodes, Issues in Designing a Multicast Routing Protocol. OS for WSN. SENSOR NETWORK ARCHITECTURE DATA DISSEMINATION: Flooding and Gossiping- Data gathering Sensor Network Scenarios –Optimization Goals and Figures of Merit, Design Principles for wsns- Gateway Concepts. Need for gateway: WSN to Internet Communication, Internet to WSN Communication –WSN Tunneling. MAC PROTOCOLS FOR SENSOR NETWORKS: Location Discovery-Quality of Sensor Networks-Evolving Standards-Other Issues- Low duty cycle and wake up concepts- The IEEE 802.15.4 MAC Protocols Energy Efficiency APPLICATION OF SENSOR NETWORKS: Geographic Routing Mobile nodes, Routing Gossiping and Agent based Unicast Forwarding-Energy Efficient Unicast- Broadcast and Multicast Geographic Routing-Mobile nodes-Security-Application Specific Support, Target detection and tracking, Contour/ edge detection-Field Sampling.

References:

1. C. S. R. Prabhu and A.P. Reddi , Bluetooth Technology; PHI.
2. Rappaport, Wireless communication, Pearson.
3. Schiller, Mobile communication, Pearson.
4. C. Y. Lee , Mobile communication, McGraw Hill.

ECE6262: NETWORK ON CHIP [3 0 0 3]

Three-Dimensional Networks-on-Chips Architectures -Resource Allocation for QoS On-Chip Communication - Networks-on-Chip Protocols-On-Chip - Processor Traffic Modeling for Networks-on-Chip. Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on- Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures- Monitoring Services for Networks-on-Chips . Energy and Power Issues in Networks-on-Chips-The CHAIN works Tool Suite: A Complete Industrial Design Flow for Networks-on-Chips. Baseline NoC Architecture – MICRO-Architecture Exploration ViChaR: A Dynamic Virtual Channel Regulator for NoC Routers- RoCo: The Row-Column Decoupled Router – A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks. Exploring Fault Tolerant Networks- on-Chip Architectures. A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures- Digest of Additional NoC MACRO-Architectural Research. ViChaR router – Wormhole router – RoCo Row Column Decoder router.

References:

1. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das, Networks -on- Chip Architectures AHolistic Design Exploration, Springer, 2009.
2.Fayezgebali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi, Networks-on-Chips theory and practice, CRC press, 2009.

ECE6263: EMBEDDED NETWORKS AND PROTOCOLS [3 0 0 3]

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols - RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming.USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets.Data flow types –Enumeration – Descriptors –PIC18 Microcontroller, USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface. Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications. Wireless sensor networks – Introduction – Applications – Network Topology – Localization – Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing. ISA/PCI Bus protocols –Firewire - A simple application with CAN - Inside the Internet protocol - Email for Embedded Systems - Data Centric routing.

References:

1. Frank Vahid, Givargis Embedded Systems Design: A Unified Hardware/Software Introduction, Wiley Publications, 2002.
2. Jan Axelson, Parallel Port Complete, Penram publications, 2011.
3. Dogan Ibrahim, Advanced PIC microcontroller projects in C, Elsevier 2008.
4. Jan Axelson Embedded Ethernet and Internet Complete, Penram publications, 2005.

PROGRAM ELECTIVE-III

ECE6264: VLSI SIGNAL PROCESSING [3 0 0 3]

Introduction to DSP systems: Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, Iteration bound, Longest path matrix algorithm, Pipelining and parallel processing of FIR filters, Pipelining and Parallel processing for low power. Retiming: Definitions and properties, Unfolding – an algorithm for unfolding, Properties of unfolding, Sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, Rank-order filters, Odd-Even merge-sort architecture, Parallel rank-order filters. Filters: Fast convolution:- Cook-Toom algorithm, Modified Cook-Toom algorithm, Pipelined and parallel recursive filters, Look-ahead pipelining in first-order IIR filters, Look-ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters. Bit-level arithmetic architectures: Parallel multipliers with sign extension, Parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, Bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement , Distributed Arithmetic fundamentals and FIR filters. Numerical strength reduction: Subexpression elimination, Multiple constant multiplication, Iterative matching, Synchronous pipelining and clocking styles, Clock skew in edge-triggered single phase clocking, Two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

References:

1. Keshab K. Parthi, *VLSI Digital Signal Processing Systems, Design and implementation*, Wiley, Inderscience, 2007.
2. U. Meyer, Baese, *Digital Signal Processing with Field Programmable Gate Arrays*, (2e), Springer, 2004.

ECE6265: NANOELECTRONIC DEVICES [3 0 0 3]

Overview: Nano electronics devices, Nano materials. Definition of Technology nodes, CMOS process flow considering cost effective and reliable process, MOS scaling theory, Issues in scaling MOS transistors: Short channel effects. Gate oxide thickness scaling trend, SiO_2 vs High-k gate dielectrics. Integration issues of high-k, Metal gate transistor: Motivation, requirements, Integration issues, Transport in nano MOSFET, SOI - PDSOI and FDSOI, Ultrathin body SOI - double gate transistors, integration issues. Vertical transistors - FinFET and Surround gate FET, Metal source/drain junctions, Requirements for Non classical MOS transistor, Germanium Nano MOSFETs: strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS, Compound semiconductors - material properties, Emerging materials for nano-device technology: Graphene, Nanotubes, nanorods and other nano structures. Nano characterization techniques (AFM and SEM), CV and IV techniques and thickness measurement techniques.

References:

1. Jean-Pierre Colinge, "*Silicon-on-Insulator Technology: Materials To VLSI"* Springer US, 2004
2. Y. Taur and T. Ning, "*Fundamentals of Modern VLSI Devices"*, Cambridge University Press, 2001.
3. Plummer, Deal, Griffin, "*Silicon VLSI Technology: Fundamentals, Practice and Modelling"*, Pearson Education India, 2001.
4. Cor Claeys Eddy Simoen*, "Germanium-Based Technologies: From Materials to Devices"* Elsevier, 2007
5. B. C.Richard, E. Charles, "*Encyclopaedia of Materials Characterization"*, Elsevier.

ECE6266: VLSI INTERCONNECTS [3 0 0 3]

Interconnects for VLSI applications: copper interconnections, method of moments, even and odd capacitances, transmission line equations- miller's theorem, Resistive interconnects as ladder network - Propagation modes in micro strip interconnects, slow wave propagations, Propagation delay. Interconnects: Parasitic resistances, capacitances and inductances approximate formulas for inductances green's function method: using method of images and Fourier integral approach- network, Inductance extraction using fast Henry-copper interconnections for resistance modelling. Interconnect Delays :Metal insulator semiconductor micro strip line- transmission line analysis for single level interconnections, transmission line analysis for parallel multilevel interconnections- analysis of crossing interconnections, parallel interconnection models for micro strip line, modelling of lossy parallel and crossing interconnects, high frequency losses in micro strip line, Expressions for interconnection delays, Active interconnects. Lumped capacitance approximation: coupled multi conductor MIS micro strip line model for single level interconnects, frequency domain level for single level interconnects, transmission line level analysis of parallel multi-level interconnections.

References:

1. H B Bakog Lu, Circuits, *Interconnections and packaging for VLSI*, Addison Wesley, 1990.
2. Nurmi J, Tenhumen H, Isoaho J, Jantsch A, *Interconnect Centric design for advanced SOC and NOC*, Springer,2004.
3. C K Cheng, J Lillis, S Lin, N Chang, *Interconnect analysis and synthesis*, Wiley,2008.

ECE6267: MOS DEVICE MODELING [3 0 0 3]

Introduction: Fermi-Dirac Statistics, Carrier concentration, Fermi level at equilibrium, recombination, and Carrier transport in silicon – drift current, diffusion current. P-N junction, built-in potential, electric field, current-voltage characteristics, band theory of solids, carrier transport mechanism.PN Junction Diode: PN Junction under thermal equilibrium under applied bias, Transient Analysis, Injection and Transport model, Diode small signal and large signal model. MOS Operation: Ideal MOS diode, Effects of mobile Ionic charges, Oxide charges and Interface states, C-V Characteristics, Threshold voltage of MOSFET, Bulk charge model, square law method (Level 1 is SPICE), Level3 model in SPICE.MOS Effects: Effect of Gate voltage on carrier mobility, Effect of Drain voltage on carrier mobility, Channel length modulation, Breakdown and punch through, Sub-threshold current, Short channel effects., Meyer's model, Small signal model. MOS Scaling: Scaling of MOSFETs – constant-voltage scaling, constant-field scaling. Short-channel MOSFETs – short-channel effects, velocity saturation, channel length modulation, source-drain series resistance, DIBL, GIDL. MOS Modelling: Basic modelling, SPICE Level-1, 2 and 3 models, BSIM model, EKV model, PSP model, Short channel effects, Equivalent circuit representation of MOS transistor, High frequency behaviour of MOS transistor and A.C small signal modelling.

References:

1. N. DasGupta and A. DasGupta, *Semiconductor Devices Modelling and Technology*, PHI, 2004.
2. B. G. Streetman and S. Banarjee, *Solid State Electronic Devices*, PHI,2004.
3. A. B. Bhattacharyya, *Compact MOSFET Models for VLSI Design*, John Wiley & Sons Inc., 2009.

ECE6268: ROBOTICS AND CONTROL [3 0 0 3]

Introduction and Mathematical Representation of Robots: Brief History of Robotics, Types of Robots, Technology of Robots, Basic Principles in Robotics. Position and Orientation of a Rigid Body, Transformation Between Coordinate Systems, Representation of Joints, Representation of Links Using Denavit–Hartenberg Parameters, Link Transformation Matrices, examples. Kinematics of Serial Manipulators: Degrees of Freedom of a Manipulator, Direct Kinematics of Serial Manipulators, Invers e Kinematics of Serial Manipulators, Manipulator With Non-intersecting Wrist, Inverse Kinematics of a General 6R Robot, Inverse Kinematics for Manipulators With $n < 6$, Inverse Kinematics of Redundant Manipulators, Solution Methods for Non-linear Equations, examples. Kinematics of Parallel Manipulators: Degrees of Freedom, Loop-closure Constraint Equations, Direct Kinematics of Parallel Manipulators, Direct Kinematics of Stewart–Gough Platform, Mobility of Parallel Manipulators, Inverse Kinematics of Parallel Manipulators, examples. Velocity Analysis and Statics of Manipulators: Linear and Angular Velocities of a Rigid Body, Linear and Angular Velocities of Links in Serial Manipulators, Serial Manipulator Jacobian, Parallel manipulator Jacobians, Singularities of Serial and Parallel Manipulators, Statics of Serial Manipulators, Statics of Parallel Manipulators, Singularity in Force Domain, Resolution of Redundancy at Velocity Level, examples. Dynamics of Manipulators: Inertia of a Link, The Lagrangian Formulation, 2R manipulator, Dynamic Equations in Cartesian Space, Inverse Dynamics of Manipulators, Simulation of Equations of Motion, Recursive Formulations of Dynamics of Manipulators, Newton–Euler Formulation for Inverse Dynamics, Algorithms for Forward Dynamics, Recursive Algorithms for Parallel Manipulators, examples.

References:

1. Ashitava Ghosal “Robotics Fundamental Concepts and Analysis”, illustrated, OUP India, 2006.
2. R K Mittal and I. J. Nagrath, “Robotics and Control”, Tata McGraw-Hill Education, 2003.
3. H. Asada and J. J. Slotine. Robot Analysis and Control. New York, NY: Wiley , 1986.
4. M. Spong, M. Vidyasagar, S. Hutchinson, Robot Modeling and Control, Wiley & Sons, 2005.
5. John J. Craig, Introduction to Robotics: Mechanics and Control, Addison-Wesley Publishing Company, 3rd Edition, 2003.

ECE6269: AUTOTRONICS [3 0 0 3]

Fundamental of automotive electronics: current trends in modern automobiles, open loop and closed loop systems, components for electronic engine management, electronic management of chassis system, vehicle motion control. Sensors and actuators: introduction, basic sensor arrangement, types of sensors such as - oxygen sensors, crank angle position sensors - fuel metering / vehicle speed sensor and detonation sensor - altitude sensor, flow sensor. Throttle position sensors, solenoids, stepper motors, and relays. Electronic fuel injection and ignition systems: introduction, feed back carburetor systems (fbc) throttle body injection and multi-port or point fuel injection, fuel injection systems, injectionsystem controls, advantages of electronic ignition systems, types of solid state ignition systems and their principle of operation, contact less electronic ignition system, electronic spark timing control. Automotive electric and electronic systems: electrical circuit components: wiring circuits, printed circuits circuit breaker, symbols and wiring diagrams, basic electrical diagnosis and tests. Lights, safety, driver information and control devices: fiber-optic and computer controlled lighting, horn and horn relay, vehicle security systems: seat belts, air bags, driver information and controls: instrument panel, speedometer and odometer speed control, head Up Display, Networks and Multiplexing, Electronic Navigation systems, Cruise control systems.

References:

1. Crouse. W.H., Automobile Electrical equipment, McGraw Hill Book Co Inc., New York, 1955.
2. Crouse. W.H.., Automotive Mechanics, McGraw Hill Education Private Limited, 2006.
3. Bechtold, Understanding Automotive Electronic, SAE, 1998.
4. William B.Riddens, Understanding Automotive Electronics, 5th Edition, Butterworth, Heinemann Woburn, 1998.

ECE6270: INDUSTRIAL AUTOMATION [3 0 0 3]

Computer based control: implementing control system using computer or microprocessor; computer based controller: hardware configuration and software requirements. Distributed control system: meaning and necessity of distributed control; hardware components of dcs; dcs software. Introduction programmable logic controller (plc): what is plc? Plc versus microprocessor/microcontroller/computer, advantages and disadvantages of plc, architecture and physical forms of plc. Basic plc functions: registers: holding, input and output registers; timers and timer functions; counters and counter functions. Intermediate plc functions: arithmetic functions: addition, subtraction, multiplication, division and other arithmetic functions; number comparison and conversion. Data handling functions of plc: skip function and applications; master control relay function and applications; jump with non-return and return; data table, register and other move functions. Bit functions of plc: digital bit functions and applications; sequencer functions and applications. Advanced functions of plc: analog input and output functions, analog input and output modules, analog signal processing in plc; pid control function, network communication function. Plc programming: plc programming languages, ladder programming, mnemonic programming and high level language programming. Scada: supervisory control versus distributed control; layout and parts of scada system, detailed block schematic of scada system; functions of scada system: data acquisition, monitoring, control, data collection and storage, data processing and calculation, report generation; mtu: functions, single and dual computer configurations of mtu; rtu: functions, architecture / layout; mtu-rtu communication and rtu-field device communication.

References:

1. Johnson CD, Process Control Instrumentation Technology, Prentice Hall.
2. Webb JW and Reis RA, Programmable Logic Controllers, Prentice Hall.
3. Hackworth JR and Hackworth FD, "Programmable Logic Controllers," Pearson Edition.
4. Boyer SA, Supervisory Control and Data Acquisition (SCADA), International Society of Automation.

ECE6271: MEMS [3 0 0 3]

Overview of MEMS & Microsystems: MEMS & Microsystems, Typical MEMS and Micro system products features of MEMS, The multidisciplinary nature of Microsystems design and manufacture, Applications of Microsystems in automotive industry, health care industry, aerospace industry, industrial products, consumer products and telecommunications. Scaling Laws in Miniaturization: Introduction to scaling, scaling in geometry, scaling in rigid body dynamics, scaling electrostatic forces, electromagnetic forces, electricity, scaling in fluid mechanics & heat transfer. Transduction Principles in MEMS & Microsystems: Introduction, Micro sensors, thermal radiation, mechanical, magnetic and biosensors, Micro actuation, MEMS with micro actuators. Microsystems Fabrication Process: Introduction, Photolithography, Ion-implantation, diffusion, oxidation, CVD, PVD, etching and materials used for MEMS, Some MEMS fabrication processes: surface micro-machining, bulk micromachining, LIGA process, LASER micro machining, MUMPS, FAB-less fabrication. Micro System Design and Modeling: Introduction, Design considerations: Process design, Mechanical design, Modeling using CAD tools: ANSYS / Multiphysics or Intellisuite or MEMS CAD, Features and Design considerations of RF MEMS, Design considerations of Optical MEMS (MOEMS), Design and Modeling: case studies - i) Cantilever beam ii) Micro switches iii) MEMS based SMART antenna in mobile applications for maximum reception of signal in changing communication conditions and iv) MEMS based micro mirror array for control and switching in optical communications. Micro system packaging: Over view of mechanical packaging of microe lectronics micro system packaging, Interfaces in micro system packaging, Packaging technologies.

References:

1. Tai — Ran Hsu, *MEMS and Micro Systems: Design and Manufacture*, Tata McGraw , 2002.
2. Boca Raton, *MEMS and NEMS: Systems, Devices and Structures*, CRC Press, 2002.
3. J. W. Gardner and V. K. Vardan, *Micro Sensors MEMS and SMART Devices*, John Wiley, 2002
4. N. Maluf, *Introduction to Micro Mechanical Systems Engineering, Artech House*, Norwood, MA, 2000.

ECE6272: MICROCONTROLLER AND EMBEDDED SYSTEMS- II [3 0 0 3]
Introduction to Computing, The PIC Microcontrollers: History and Features, PIC Architecture & Assembly Language Programming, Branch, Call, and Time Delay Loop, PIC I/O Port Programming, Arithmetic, Logic Instructions, and Programs, Bank Switching, Table Processing, Macros, and Modules, PIC Programming in C, PIC18F Hardware Connection and ROM Loaders, PIC18 Timer Programming in Assembly and C, PIC18 Serial Port Programming in Assembly and C, Interrupt Programming in Assembly and C, LCD and Keyboard Interfacing, ADC, DAC, and Sensor Interfacing, Using Flash and EEPROM Memories for Data Storage, CCP and ECCP Programming, SPI Protocol and DS1306 RTC Interfacing, Motor Control: Relay, PWM, DC, and Stepper Motors.

References:

1. Muhammad Ali Mazidi, Danny Causey, et al. , PIC Microcontroller and Embedded Systems using assembly and C, Pearson Education India, 2008.
2. John B. Peatman, Design with PIC Micro controller, Pearson Education, 1988.
3. Dogan Ibrahim, PIC Microcontroller Projects in C: Basic to Advanced 2nd Edition, Newnes, 2014.
4. Muhammad Ali Mazidi, Rolin D. McKinlay, PIC Microcontroller, Danny Causey Pearson Education.
5. Tim Wilmshurst, Designing Embedded Systems with PIC Microcontrollers: Principles and Applications 2nd Edition, Newnes, 2009.

ECE6232 EMBEDDED SYSTEM DESIGN LAB - II

Design of microcontroller-based embedded systems; interfacing from both a hardware and software perspective; and applications, including audio, data acquisition, and communication systems. Students should be able to design embedded systems including hardware/software interfaces for devices like LCD displays, motors, keyboards, analog sensors and speakers. Furthermore, students will be able to deploy these systems into the IoT environment.

ECE6234 IC DESIGN LAB LAB [0 0 2 1]

This lab give exposure to simulation of various digital & analog circuits using CMOS and various other logic families using HSPICE & SYNOPYS software's. This lab also aims at designing of the circuits with the given design constraint. Virtual Fabrication for various nano devices using TCAD tools is also a part of the lab.

ECE6233 MINOR PROJECT [0 0 2 1]
Students are required to undertake innovative and research oriented projects (academics and industry - based) which not only reflect their knowledge gained in the first and/or second semester, but also reflects additional knowledge gained from their own effort. Each student has to submit to the department a project report in prescribed format after completing the work for end-term evaluation. The final evaluation and viva- voice will be after submission of the report. Each student has to make a presentation on the work carried out for project evaluation. The end semester evaluation will be done by a monitoring committee constituted by the head of department.

Open Elective

ECE6080: INTRODUCTION TO CMOS VLSI [3 0 0 3]

Basic MOS Technology: Introduction to VLSI, VLSI Design Flow, Full custom, semi- custom design, Enhancement and depletion mode MOS transistors. NMOS fabrication. CMOS fabrication. MOS Transistor Theory: Introduction, MOS device current equations, Scaling, CMOS inverter-DC characteristics, static load MOS inverters. Design of Inverters. Combinational Circuit using CMOS logic families: Design of Logic gates and various combinational circuits using CMOS, Pseudo NMOS, Transmission Gate & Pass Transistors. Sequential Circuit using CMOS logic families: Design of flip flops and various sequential circuits using CMOS, Domino, Dynamic, zipper, NORA Circuits. CMOS subsystem design processes: General considerations, process illustration, ALU subsystem, adders, multipli ers, memory elements, memory cell arrays

References:

1. S.M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, TMH, 2003.
2. N. Weste & K. Eshragian, Principles of CMOS VLSI Design: A System Perspective, Pearson, 2000.
3. J. M. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall, 2003.
4. D. A Pucknell and K. Eshraghian, Basic VLSI Design, PHI, 2005.

Third & Fourth Semester

ECE7070: DISSERTATION

Students are required to undertake innovative and research oriented projects, which not only reflect their knowledge gained in the previous two semesters but also reflects additional knowledge gained from their own effort. The project work can be carried out in the institution/ industry/ research laboratory or any other competent institutions. The duration of project work should be a minimum of 36 weeks. There will be a mid- term evaluation of the project work done after about 18 weeks. An interim project report is to be submitted to the department during the mid-term evaluation. Each student has to submit to the department a project report in prescribed format after completing the work. The final evaluation and viva-voice will be after submission of the report. Each student has to make a presentation on the work carried out, before the departmental committee for project evaluation. The mid-term & end semester evaluation will be done by the departmental committee including the guides.